

ABSTRACT

When a high-voltage, such as from an ESD pulse, is placed across a silicon controlled rectifier, which includes an NPN transistor and a PNP  
5 transistor that is connected to the NPN transistor, the likelihood of punch through occurring between two regions of the rectifier is substantially reduced by forming the emitter of one transistor adjacent to the tails of the sinker down region of the other transistor.

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